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Implementation Of Convolutional Encoder And
Implementation of convolutional

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Viterbi and Viterbi decoder using VHDL Abstract: This work focuses on the realization of convolutional encoder and adaptive Viterbi decoder (AVD) with a constraint length, K of 3 and a code rate (k/n) of $1/2$ using field-programmable gate array (FPGA) technology.

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Implementation of convolutional encoder and Viterbi ...

Convolutional codes are non blocking codes that can be designed to either error detecting or correcting.

Convolution coding has been used in communication systems including

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Viterbi deep space communication and wireless communication. At the receiver end the original message sequence is obtained from the received data using Viterbi decoder.

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Convolutional codes are employed to implement FEC .It take a single or multi-bit input and generate a matrix of encoded outputs. Figure 2.1.1:Convolutional Encoder of code rate $\frac{1}{2}$. Above shows block diagram of $\frac{1}{2}$ rate convolutional encoder. Using this let us draw truth table. Trellis

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Viterbi Diagram: Trellis diagram can be obtained by using above truth table. Firstly write the

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The process of adding this redundant information is known as channel

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Viterbi coding. Convolutional codes operate on serial data, one or a few bits at a time. Convolutional encoding with Viterbi decoding is a FEC technique that is particularly suited to a channel in which mainly Additive White Gaussian Noise (AWGN) corrupts the transmitted signal.

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Convolutional encoder example |
Convolutional coding

The 1 in the generator polynomial indicates the connections and zero indicates no connections between the stage and the modulo 2 adder. The figure below illustrates a simple

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Viterbi convolutional coder with $k=1, K=3,$
 $n=3, g_1(n) = (1\ 0\ 1), g_2(n) = (1\ 1\ 1),$
 $g_3(n) = (0\ 1\ 1)$ and $R=1/2$. Fig 2.2
Convolutional Encoder.

Implementation of Reconfigurable
Convolutional Encoder and ...

Viterbi decoding is the best technique

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Viterbi for decoding the convolutional codes. Convolution encoder and Viterbi decoder are widely used in many communication systems due to the excellent error control performance. This work deals with the design and implementation of convolution encoder and Viterbi decoder using

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Design and Implementation of Convolutional Encoder and ...

The most important aspect dealt in this paper is the implementation of Convolution encoder and Viterbi decoder on FPGA platform by

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reducing the area and henceforth improving the speed performances. In general digital/wireless communication systems were designed on Digital Signal Processors (DSPs).

An Efficient FPGA Implementation of

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Viterbi Convolutional Encoder ...

Methods: The study proposes convolutional encoder with 1/2 code rate and constrained length of 3. An improved architecture which optimizes critical path delay is proposed to achieve higher speeds. The design is carried out in MATLAB.

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The simulation of proposed architecture is done using XILINX 14.1 and implementation is done using FPGA SPARTAN 3AN.

Design and Implementation of High Speed Viterbi Decoder ...

The convolutional encoder is based on

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a rate $1/2$ mother convolutional code with constraint length $K = 7$ corresponding to 64 trellis states. The input serial stream is encoded in two branch X and Y with the following polynomial: X output (171 octal) Y output (133 octal) Figure 2 reports the encoder architecture. Figure 2 –

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DVB-S Convolutional Encoder Architecture . VHDL implementation of Convolutional Encoder . Figure 2 shows the classical architecture of a convolutional encoder.

How to implement convolutional encoder in VHDL - Surf-VHDL

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In telecommunication, a convolutional code is a type of error-correcting code that generates parity symbols via the sliding application of a boolean polynomial function to a data stream. The sliding application represents the 'convolution' of the encoder over the data, which gives rise to the term

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Viterbi 'convolutional coding'. The sliding nature of the convolutional codes facilitates trellis ...

Convolutional code - Wikipedia

ABSTRACT: This paper represents the SDR implementation of convolutional encoder and Viterbi decoder. In this

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Viterbi paper there are two parts where one part is based on the VHDL simulation of encoder and decoder and second part is based on hardware, in which all these simulations are implemented on SDR (an FPGA). This paper has taken random

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Vol.3, Issue 5, May 2014 SDR

Implementation of ...

In this paper, a modified FPGA scheme for the convolutional encoder and Viterbi decoder based on the IEEE 802.11a standards of WLAN is presented in OFDM baseband processing systems. The proposed

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Viterbi design supports a generic, ro-bust and configurable Viterbi decoder with constraint length of 7, code rate of 1/2 and decoding depth of 36 symbols.

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Viterbi Design Simulation and

Implementation Timing Results This research presents the implementation of Convolutional encoder- Viterbi decoder architecture on XC3S500E chip [10], using Spartan-3E FPGA Starter Kit, Project Navigator 8.2i Software (for modeling, verification

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Viterbi (and implementation) and Model Sim XE II/ Starter 5.8c Software which is used for timing simulation.

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In order to simplify the hardware design and reduce the resource

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Viterbi requirements, this paper proposes a novel implementation of a convolutional auto-encoder (CAE) in a field programmable gate array...

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126 FPGA Design and Implementation

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Viterbi of a Convolutional Encoder and a Viterbi Decoder Based on 802.11a for OFDM development the VA operation problem has been solved to a great extent. This makes the Viterbi the most extensive, robust and capable decoding algorithm when the value of m is less than or equal to 10.

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Implementation of convolutional encoder and Viterbi decoder using VHDL Abstract: This work focuses on the realization of convolutional encoder and adaptive Viterbi decoder

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(AVD) with a constraint length, K of 3 and a code rate (k/n) of $1/2$ using field-programmable gate array (FPGA) technology. Implementation of convolutional encoder and Viterbi ...

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In this paper, a modified FPGA scheme for the convolutional encoder and Viterbi decoder based on the IEEE 802.11a standards of WLAN is presented in OFDM baseband processing systems. The proposed design supports a generic, robust and configurable Viterbi decoder with

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Viterbi constraint length of 7, code rate of 1/2 and decoding depth of 36 symbols.

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A Convolutional Encoder with 5-bit input and 2-bit output The

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Viterbi convolutional encoder is effectively a 5-bit shift register with bits $[x_0, x_1, x_2, x_3, x_4]$ where x_0 is the new incoming bit and x_4 is the oldest bit in the register that is shifted out on each cycle. For PSK31 each bit will come in at 31.25Hz. Note, here is a post on Convolutional Decoding.

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PSK31 Convolutional Encoder
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